REMARKS

No claims have been amended, added or cancelled. Therefore, claims 1-27 remain pending in the application. Reconsideration is respectfully requested in light of the following remarks.

Section 102(b) Rejection:

The Examiner rejected claims 1-3, 5-10, 12-14, 16-21, 23, 24 and 27 under 35 U.S.C. § 102(b) as being anticipated by Tredennick et al. (U.S. Patent 4,338,661) (hereinafter "Tredennick"). Applicants respectfully traverse this rejection for at least the following reasons.

Regarding claim 1, contrary to the Examiner's assertion, Tredennick fails to teach or suggest *a microcode ROM, wherein a row in the microcode ROM stores a plurality of groups of microcode operations*. The Examiner cites column 15, lines 33-34 and 36-37 as teaching these limitations. These passages describe a micro ROM 72 containing 544 microwords, each having 17 bits, which are addressed by a 10-bit output of address selection block 64. There is nothing in this citation, or elsewhere in Tredennick, that teaches or suggests that these microwords comprise groups of microcode operations, or that a row in Tredennick's microcode ROM stores a plurality of groups of microcode operations.

Similarly, Tredennick fails to teach or suggest *wherein a group of the plurality of groups of microcode operations is comprised in a microcode routine*. The Examiner cites column 1, lines 55-56 as teaching this limitation. However, this passage discloses only a data processor having a control store containing a plurality of microinstruction routines for implementing instructions received by the data processor. It says nothing about how these routines are stored within the ROM, or about them comprising a group of microcode operations (from among a plurality of such groups). There is nothing in Tredennick that teaches or suggests this limitation.

Tredennick also fails to teach or suggest *wherein the row stores an associated control sequence for each of the plurality of groups of microcode operations.* The Examiner cites column 15, lines 52-55 and 59-66 as teaching this limitation. These passages describe two formats for microwords. In a microword of a conditional branch type (type II), bits 7 thru 14 comprise a next micro ROM base address (NMBA) for the micro and nano control stores, which is augmented by 2 additional bits supplied by branch control logic in order to specify the next address for the control stores. In microwords having format type I, bits 2 and 3 comprise a type field (TY) which specifies the source of the next address for the control stores as being from one of the 3 possible addresses provided by the instruction register sequence decoder or from a direct branch address provided by bits 5 thru 14 of the microword. Thus, these passages disclose that information stored in each microword is used in determining the next address for the control stores. They do not describe a control sequence being associated with a group of instructions comprising a row in the microcode, as in Applicants' claimed invention. There is nothing in these passages or elsewhere that teaches or discloses **a row** storing an associated control sequence for each of the plurality of groups of microcode operations stored in the row.

Further regarding claim 1, Tredennick fails to teach or suggest *a control sequence logic unit coupled to the microcode ROM, wherein in response to accessing the group of microcode operations comprised in the microcode routine, the control sequence logic unit is configured to use the control sequence associated with the group of microcode operations to identify an other row storing one or more next groups of microcode operations comprised in the microcode routine.* The Examiner cites column 15, lines 37-40 as teaching this limitation ("it selects the next line of the ROM, which is output from the microcode ROMs as shown in column 15, lines 52-55 and 59-66.") First, as discussed above, Tredennick does not disclose a control sequence associated with a group of instructions. In addition, column 15, lines 37-40 merely describes that the micro ROM is addressed by the 10-bit output of address selection block 64. Furthermore, the Examiner's statement "it selects the next line of the ROM, which is output from the

microcode ROMs as shown in column 15, lines 52-55 and 59-66" has no basis in Tredennick. As discussed above, column 15, lines 52-55 and 59-66 describes how the next address for the control stores is determined for microwords having type I and type II formats. None of these descriptions includes identifying an other row storing one or more next groups of microcode operations comprised in the microcode routine. Tredennick says nothing about the next address identifying another row, about another row storing one or more groups of microcode operations, or about another row storing one or more next groups of microcode operations comprised in the (same) microcode routine, as in Applicants' claimed invention.

Applicants remind the Examiner that anticipation requires the presence in a single prior art reference disclosure of each and every limitation of the claimed invention, arranged as in the claim. M.P.E.P 2131; *Lindemann Maschinenfabrik GmbH v. American Hoist & Derrick Co.*, 221 USPQ 481, 485 (Fed. Cir. 1984). The identical invention must be shown in as complete detail as is contained in the claims. *Richardson v. Suzuki Motor Co.*, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989). As discussed above, Tredennick fails to disclose many of the limitations of Applicants' claim 1. Therefore, Tredennick cannot be said to anticipate claim 1.

For at least the reasons above, the rejection of claim 1 is unsupported by the cited art and removal thereof is respectfully requested.

Claims 12 and 23 include limitations similar to claim 1, and so the arguments presented above apply with equal force to these claims, as well.

Regarding claim 27, contrary to the Examiner's assertion, Tredennick fails to teach or suggest *a microcode ROM, wherein a row in the microcode ROM stores a plurality of groups of microcode operations and wherein the row stores an associated control sequence for each of the plurality of groups*. The Examiner again cites column 15, lines 33-34, 36-37, 52-55, and 59-66 as teaching these limitations. However, as discussed above regarding claim 1, Tredennick does not teach or suggest a row in the

microcode storing groups of microcode operations and a control sequence associated with each of the groups.

Further regarding claim 27, Tredennick fails to teach or suggest *means for accessing a control sequence associated with one of the plurality of groups of microcode operations and responsively accessing a next group of microcode operations stored in the microcode ROM.* The Examiner again cites "Column 15, lines 37-40, it selects the next line of the ROM, which is output from the microcode ROMs as shown in column 15, lines 52-55 and 59-66." However, as discussed above regarding claim 1, Tredennick does not teach or suggest groups of microcode operations stored in a row or a control sequence associated with a group of microcode operations, and therefore, does not teach or suggest accessing such a sequence or responsively accessing a next group of microcode operations stored in the microcode ROM. Therefore, Tredennick cannot be said to anticipate claim 27.

For at least the reasons above, the rejection of claim 27 is unsupported by the cited art and removal thereof is respectfully requested.

Regarding claim 2, contrary to the Examiner's assertion, Tredennick fails to teach or suggest *at least one of the plurality of groups of microcode operations stored in the row is part of a different microcode routine.* The Examiner cites Figure 11 and column 19, lines 52-55 as teaching this limitation. This passage and figure illustrate how only one input address may reference a particular (single) microword location but one, two, or four input addresses may reference the same (single) nanoword location in order to reduce the size of the control store (see, e.g., column 19, lines 13-34.) This has nothing to do with whether one of a plurality of groups of microcode operations stored in a row is part of a different microcode routine. As discussed above regarding claim 1, Tredennick does not teach or suggest a microcode ROM organized according to the rows, routines, and groups of Applicants' claimed invention.

For at least the reasons above, the rejection of claim 2 is unsupported by the cited art and removal thereof is respectfully requested.

Claim 13 includes limitations similar to claim 2, and so the arguments presented above apply with equal force to this claim, as well.

Regarding claim 3, contrary to the Examiner's assertion, Tredennick fails to teach or suggest *wherein the control sequence logic unit is configured to identify which of a plurality of groups of microcode operations stored in the other row of the microcode ROM are comprised in the microcode routine based on information contained in the control sequence associated with the group of microcode operations stored in the row.* The Examiner cites column 15, lines 52-55 and 59-66, "which defines which row and position the next group is located," as teaching these limitations. However, as discussed above, this citation does not teach identifying a row and position for a next group of microcode operations. Instead, this passage describes how the next address (which is clearly not the same as "a row and position") is determined for an individual microword having a type I or type II format. As discussed above regarding claim 1, Tredennick does not teach or suggest a microcode ROM organized according to the rows, routines, and groups of Applicants' claimed invention. Furthermore, there is nothing in the Examiner's citation or elsewhere in Tredennick that teaches or suggests that identifying the next address (or "a row and position") has anything to do with identifying "which of a plurality of groups of microcode operations stored in the other row of the microcode ROM are comprised in the microcode routine," as recited in claim 3.

For at least the reasons above, the rejection of claim 3 is unsupported by the cited art and removal thereof is respectfully requested.

Claim 14 includes limitations similar to claim 3, and so the arguments presented above apply with equal force to this claim, as well.

Regarding claim 5, contrary to the Examiner's assertion, Tredennick fails to teach or suggest *wherein if the group of microcode operations comprises at least one branch operation, the control sequence logic unit is configured to identify the next group of microcode operations in the microcode routine dependent on a branch prediction as well as the control sequence associated with the group of microcode operations.* The Examiner cites column 15, lines 49-55 ("teach a microcode instruction for branches") and column 17, lines 29-32 ("show that the outcome either way will be in the same row specified by the control sequence") as teaching these limitations. The Examiner's citation in column 17 states, "Thus, two microwords which serve as alternate destinations for a particular conditional branch type microword must be placed in the same logical row of the micro ROM." Applicants assert that this citation does not describe identifying the next group of microcode operations in a microcode routine, but instead describes two alternate (individual) addresses that may be the destination of a branch operation. Furthermore, the Examiner's remarks appear to teach away from identifying the next group of operations dependent on a branch prediction. Instead, they imply that no branch prediction is necessary (or performed) because "the outcome either way will be in the same row." In fact, branch prediction is not disclosed in Tredennick. Finally, Applicants' claim 5 does not recite identifying a row to be accessed after a conditional branch, as the Examiner suggests, but instead recites, "the control sequence logic unit is configured to identify the next group of microcode operations in the microcode routine..." which Tredennick clearly does not disclose. Therefore, Tredennick cannot be said to anticipate claim 5.

For at least the reasons above, the rejection of claim 5 is unsupported by the cited art and removal thereof is respectfully requested.

Claims 16 and 24 include limitations similar to claim 5, and so the arguments presented above apply with equal force to these claims, as well.

Regarding claim 6, contrary to the Examiner's assertion, Tredennick fails to teach or suggest *wherein the microcode ROM is divided into a plurality of segments, wherein a*

same number of groups of microcode operations is stored in each row of a given one of the plurality of segments, and wherein each row in the given one of the plurality of segments stores a different number of groups of microcode operations than each row in each other one of the plurality of segments. The Examiner cites column 19, lines 22-27 as teaching this limitation ("for each row, the address may represent one, two, four, or up to eight different groups. So there are segments in the sense that some lines can contain a different number of groups than the other lines.") The Examiner has misquoted column 19. The Examiner's citation states, "Each word line in the micro ROM is represented by only one input address. Each word line in the nano ROM however may represent one, two, or four possible different input addresses. In the preferred embodiment of the data processor, a word line in the nano ROM may represent as many as eight different input addresses." However, "a word line" in Tredennick is not a row in the microcode ROM that stores a plurality of groups of microcode operations, as in Applicants' claimed invention. Instead, "a word line" selects a single microword and/or a single nanoword from the micro ROM and nano ROM, respectively. (See, e.g., column 19, lines 13-22: "the same address is presented to the decoders of both the micro ROM and the nano ROM. For any input address, there will be no more than one word line in each ROM which remains high. The line which remains high will cause the appropriate output value to be generated as the micro ROM output word and the nano ROM output word according to the coding at the intersection of the selected word line and the output columns." There is nothing in Tredennick that teaches or suggest the microcode ROM is divided into a plurality of segments having the limitations recited in claim 6 ("wherein a same number of groups of microcode operations is stored in each row of a given one of the plurality of segments, and wherein each row in the given one of the plurality of segments stores a different number of groups of microcode operations than each row in each other one of the plurality of segments.") Therefore, Tredennick cannot be said to anticipate claim 6.

For at least the reasons above, the rejection of claim 6 is unsupported by the cited art and removal thereof is respectfully requested.

Claim 17 includes limitations similar to claim 6, and so the arguments presented above apply with equal force to this claim, as well.

Similarly, Tredennick fails to teach or suggest the limitations of claims 7-9, which recite, in part, *wherein groups of microcode operations stored in a same one of the plurality of segments have a same maximum width* (claim 7), *wherein groups of microcode operations stored in one of the plurality of segments have a maximum width that is different from a maximum width of groups of microcode operations stored in another one of the plurality of segments* (claim 8), and *wherein one of the plurality of segments stores one group of microcode operations and one associated control sequence per row* (claim 9.) The Examiner cites column 19, lines 22-27 as teaching all of these limitations. However, as discussed above, this citation has nothing to do with a plurality of segments in a microcode ROM, much less with such segments having the limitations recited in claims 7-9. Therefore, Tredennick cannot be said to anticipate these claims.

For at least the reasons above, the rejection of claims 7-9 is unsupported by the cited art and removal thereof is respectfully requested.

Claims 18-20 include limitations similar to claims 7-9 and so the arguments presented above apply with equal force to these claims, as well.

Regarding claim 10, contrary to the Examiner's assertion, Tredennick fails to teach or suggest *wherein the control sequence logic unit is configured to identify a position of one or more groups of microcode operations and a position of one or more control sequences dependent on which of the plurality of segments of the microcode ROM stores the one or more groups of microcode operations*. The Examiner cites column 15, lines 52-55 and 59-66, "which defines which row and position the next group is located," as teaching this limitation. However, as discussed above, this citation this citation does not teach identifying a row and position for a next group of microcode operations. Instead, this passage describes how the next address (which is clearly not the same as "a row and position") is determined for an individual microword having a type I or type II

format. As discussed above, Tredennick does not teach or suggest a microcode ROM organized according to the rows, routines, groups, and segments of Applicants' claimed invention, and clearly does not teach identifying a position of one or more groups of microcode operations and control sequences dependent on which of a plurality of segments stores the one or more groups of microcode operations. Therefore, Tredennick clearly does not anticipate claim 10.

For at least the reasons above, the rejection of claim 10 is unsupported by the cited art and removal thereof is respectfully requested.

Claim 21 includes limitations similar to claim 10, and so the arguments presented above apply with equal force to this claim, as well.

Section 103(a) Rejection:

The Examiner rejected claims 4, 11, 15, 25 and 26 under 35 U.S.C. § 103(a) as being unpatentable over Tredennick in view of Yoshida (U.S. Patent 5,761,470). Applicants respectfully traverse this rejection for at least the following reasons.

Regarding claim 4, contrary to the Examiner's assertion, Tredennick in view of Yoshida fails to teach or suggest *wherein if fewer than all of a plurality of groups of microcode operations stored in the other row of the microcode ROM are comprised in the microcode routine, the control sequence logic unit is configured to substitute NOPs for the microcode operations comprised in the groups not comprised in the microcode routine when outputting the row to the scheduler.* The Examiner submits that Tredennick teaches the microprocessor of claim 3, which Applicant traverses above. The Examiner admits that Tredennick fails to teach the above-referenced limitation of claim 4, and relies on Yoshida to teach it. Yoshida teaches of a VLIW machine, which exploits parallelism by executing multiple instructions simultaneously. Yoshida teaches that if the conventional VLIW machine cannot execute an instruction from the word in parallel, it

inserts a NOP in its place, as it has to execute some instruction (column 1, lines 51-56). The Examiner submits that, "Given the advantage of higher speed though parallelism, one of ordinary skill in the art at the time the invention was made would have converted Tredennick's invention to operate in a parallel fashion such as a VLIW machine to increase the speed and performance."

Applicants remind the Examiner that, as stated in the MPEP §2143.01 "If the proposed modification or combination of the prior art would change the principle of operation of the prior art invention being modified, then the teachings of the references are not sufficient to render the claims *prima facie* obvious. *In re Ratti* , 270 F.2d 810, 123 USPQ 349 (CCPA 1959). . ." (*emphasis added*). Converting Tredennick's invention to operate in a parallel fashion would clearly (and dramatically) change the principle of operation of his invention.

Applicants also remind the Examiner that to establish a *prima facie* obviousness of a claimed invention, all claim limitations must be taught or suggested by the prior art. *In re Royka*, 490 F.2d 981, 180 U.S.P.Q. 580 (C.C.P.A. 1974), MPEP 2143.03. Applicants assert that converting Tredennick's invention "to operate in parallel fashion" would not necessarily result in Applicants' claimed invention. The feature described in Yoshida "if the conventional VLIW machine cannot execute an instruction from the word in parallel, it inserts a NOP in its place" refers to a VLIW processor that consumes one instruction even when there are no operations which can be executed in parallel. In this case, a number of operation fields specifying null operations (No Operation: NOP) are generated, and the amount of instruction code becomes very big. This is clearly not the same as the limitation in Applicants' claim 4, which recites "*wherein if fewer than all of a plurality of groups of microcode operations stored in the other row of the microcode ROM are comprised in the microcode routine, the control sequence logic unit is configured to substitute NOPs for the microcode operations comprised in the groups not comprised in the microcode routine when outputting the row to the scheduler,*" as Yoshida does not describe the organization of a microcode ROM at all, much less one in which groups of microcode operations are stored in particular rows. Furthermore, it is

not clear that all parallel processors necessarily include this "feature" of Yoshida, nor does the reference (or the Examiner, in his remarks) explain how this feature would be implemented in Tredennick's processor if "converted to operate in parallel fashion." Therefore, Applicants assert that Tredennick in view of Yishida fails to teach or suggest all the limitations of claim 4.

For at least the reasons above, the rejection of claim 4 is unsupported by the cited art and removal thereof is respectfully requested.

Claims 15 and 25 include limitations similar to claim 4, and so the arguments presented above apply with equal force to these claims, as well.

Similarly, Tredennick in view of Yoshida fails to teach or suggest *wherein a plurality of groups of microcode operations stored in the other row of the microcode ROM are comprised in the microcode routine and are output during a single access*, as recited in claim 11. The Examiner admits that Tredennick fails to teach this limitation, and again relies on Yoshida's VLIW machine to teach this limitation. As discussed above, the Examiner's proposed modification of the prior art would change the principle of operation of the prior art invention being modified, and thus the teachings of the references are not sufficient to render the claims *prima facie* obvious.

In addition, the Examiner's citations in Yoshida do not teach *a plurality of groups of microcode operations stored in the other row of the microcode ROM are comprised in the microcode routine and are output during a single access*. They teach that one VLIW word can specify a plurality of instructions (column 1, lines, 25-30), but they do not disclose that instructions are output during a single access, that they are stored in rows, or wherein a plurality of groups of microcode operations stored in the other row of the microcode ROM are comprised in a microcode routine.

For at least the reasons above, the rejection of claim 11 is unsupported by the cited art and removal thereof is respectfully requested.

Claims 22 and 26 include limitations similar to claim 11, and so the arguments presented above apply with equal force to these claims, as well.

CONCLUSION

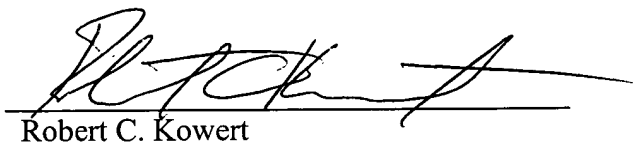
Applicants submit the application is in condition for allowance, and prompt notice to that effect is respectfully requested.

If any extension of time (under 37 C.F.R. § 1.136) is necessary to prevent the above-referenced application from becoming abandoned, Applicants hereby petition for such an extension. If any fees are due, the Commissioner is authorized to charge said fees to Meyertons, Hood, Kivlin, Kowert, & Goetzel, P.C. Deposit Account No. 501505/5500-91700/RCK.

Also enclosed herewith are the following items:

- ☒ Return Receipt Postcard
- ☐ Petition for Extension of Time
- ☐ Notice of Change of Address
- ☐ Other:

Respectfully submitted,



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